

#9
284/Amendment
J. White
4-11-02

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By: 

Date: March 6, 2002

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Francisco Pires
Applic. No. : 09/816,932
Filed : March 23, 2001
Title : Conductor Track Layer Structure and Prestage
Thereof
Examiner : Quynh-Nhu H. Vu
Group Art Unit : 2841

A M E N D M E N T

Hon. Commissioner of Patents and Trademarks,
Washington, D. C. 20231

S i r :

Responsive to the Office action dated December 6, 2001 kindly
amend the above-identified application as follows:

In the Specification:

Page 1, between lines 4 and 6, insert

-- BACKGROUND OF THE INVENTION:

FIELD OF THE INVENTION: --.

A1

Page 1, between lines 7 and 9, insert

A2

-- DESCRIPTION OF THE RELATED ART --.

Page 4, between lines 12 and 14, insert

A3

-- SUMMARY OF THE INVENTION: --.

delete lines 19-21 and insert the following

A4

-- This object is attained with a conductor track layer structure precursor stage comprising:

an electrically insulating substrate having an inner region and two opposite lateral peripheral regions;

two current lines, each extending respectively in one of the two opposite lateral peripheral regions;

a plurality of conductor tracks disposed on the inner region of the electrically insulating substrate;

a plurality of conductor track current lines connecting the plurality of conductor tracks, respectively, to one of the two current lines;

said conductor tracks being connected to one of the two current lines via a separate conductor track current line and

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cont being electrically insulated from the other of the two current lines; and

the conductor tracks inside the inner region being electrically insulated from one another.

According to another feature of the invention, the electrically insulating substrate is a flexible plastic film.

This object is further attained with a conductor track layer structure, comprising the conductor track layer structure precursor stage in which the lateral peripheral regions are removed.

According to an additional feature of the invention, the lateral peripheral regions are knocked off.--.

Page 8, above the first line, insert

A5 -- BRIEF DESCRIPTION OF THE DRAWINGS: --.

between lines 19 and 21, insert

A6 -- DESCRIPTION OF THE PREFERRED EMBODIMENT: --.

Page 14, top, change "Abstract" to -- ABSTRACT OF THE

A7 DISCLOSURE: --.

line 4, delete "CONDUCTOR TRACK LAYER SSTRUCTURE AND
PRESTAGE THEREOF".

In the Claims:

Page 12, top, change "Claims" to -- I CLAIM: --.

A8
Cancel claims 1-4.

Please Add the Following New Claims:

A9
5. A conductor track layer structure precursor stage
comprising:

an electrically insulating substrate having an inner region
and two opposite lateral peripheral regions;

two current lines, each extending respectively in one of said
two opposite lateral peripheral regions;

a plurality of conductor tracks disposed on said inner region
of said electrically insulating substrate;

a plurality of conductor track current lines connecting said
plurality of conductor tracks, respectively, to one of said
two current lines;

A9
cont
said conductor tracks being connected to one of said two
current lines via a separate conductor track current line and
being electrically insulated from the other of said two
current lines; and

said conductor tracks inside said inner region being
electrically insulated from one another.

6. The conductor track layer structure precursor stage
according to claim 5, wherein said electrically insulating
substrate is a flexible plastic film.

7. A conductor track layer structure, comprising the
conductor track layer structure precursor stage according to
claim 5 or 6 in which the lateral peripheral regions are
removed.

8. The conductor track layer structure according to claim 7,
wherein the lateral peripheral regions are knocked off.

Remarks:

Reconsideration of the application is requested.

Claims 5-8 are now in the application. Claims 1-4 have been cancelled and claims 5-8 have been added.

In deference to the requirement by the Examiner in item 1 on page 2 of the above-identified Office action, Figs. 5a and 5b have been designated with a legend "Prior Art".

In deference to the requirement by the Examiner in item 2 on page 2 of the above-identified Office action, the Examiner's suggested layout for the patent application has been adopted.

In item 4 on page 3 of the above-identified Office action, claims 1-4 have been rejected as being anticipated by Edwards (US Pat. No. 4,580,193) under 35 U.S.C. § 102(b).

The rejection has been noted. Claims 1-4 have been cancelled and claims 5-8 have been added in an effort to even more clearly define the invention of the instant application. More specifically, the new claim 5 contains the features of original claims 1 and 2. The following discussion is therefore directed to claim 5.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 5 calls for, inter alia:

two current lines, each extending respectively in one of said two opposite lateral peripheral regions;
a plurality of conductor track current lines connecting said plurality of conductor tracks, respectively, to one of said two current lines;
said conductor tracks being connected to one of said two current lines via a separate conductor track current line and being electrically insulated from the other of said two current lines.

Edwards discloses a configuration for attaching leads from several chips to bus lines on a printed circuit board.

However, in Edwards all tracks are isolated from each other and separately connected with contacting pads. On the contrary, in the invention of the instant application, the conductor tracks are connected to one of the two opposite current lines and therefore some of the tracks are connected to a common current line.

The invention of the instant application originated from a method for electrochemically depositing a layer on the various conducting tracks. Therefore, it relates to a carrier with one current lead on each of the two edges. These leads only have an auxiliary function. The conducting tracks are being connected with these current leads temporarily, and after the electrochemical deposition the connections are cut. Edwards

fails to refer to the problem of using auxiliary leads for depositing layers on conducting tracks. The conducting tracks are not connected with such leads in the edge regions of the carrier, and no cutting of the tracks is contemplated.

Clearly, Edwards does not show two current lines and the conductor tracks being connected to one of the two current lines via a separate conductor track current line, as recited in claim 5 of the instant application.

Claim 5 is, therefore, believed to be patentable over Edwards and since claims 6-8 are ultimately dependent on claim 5, they are believed to be patentable as well.

In item 5 on pages 3-4 of the above-identified Office action, claims 1-4 have been rejected as being anticipated by Janai et al. (US Pat. No. 5,541,814) under 35 U.S.C. § 102(b).

Janai et al. disclose a personalizable multi-chip carrier, wherein a plurality of crossing locations is provided with fusible links. However, Janai et al. do not show two current lines and the conductor tracks being connected to one of the two current lines via a separate conductor track current line, as recited in claim 5 of the instant application. Claim 5 is, therefore, believed to be patentable over Janai et al. and

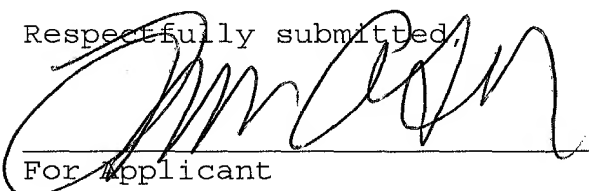
since claims 6-8 are ultimately dependent on claim 5, they are believed to be patentable as well.

In view of the foregoing, reconsideration and allowance of claims 5-8 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate a telephone call so that, if possible, patentable language can be worked out.

Please charge any fees which might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,


For Applicant

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